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APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
09/830,361	04/25/2001	Yasushi Inagaki	P279059	4952
909	7590	05/17/2004	EXAMINER DINH, TUAN T	

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ART UNIT
2827

PAPER NUMBER

DATE MAILED: 05/17/2004

Please find below and/or attached an Office communication concerning this application or proceeding.

Office Action Summary	Application No.	Applicant(s)
	09/830,361	INAGAKI ET AL.
	Examiner Tuan T Dinh	Art Unit 2827

-- The MAILING DATE of this communication appears in the cover sheet with the correspondence address --
Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If the period for reply specified above is less than thirty (30) days, a reply within the statutory minimum of thirty (30) days will be considered timely.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

- 1) Responsive to communication(s) filed on 09 April 2004.
- 2a) This action is FINAL. 2b) This action is non-final.
- 3) Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

- 4) Claim(s) 1-9 is/are pending in the application.
- 4a) Of the above claim(s) _____ is/are withdrawn from consideration.
- 5) Claim(s) 6-9 is/are allowed.
- 6) Claim(s) 1-5 is/are rejected.
- 7) Claim(s) _____ is/are objected to.
- 8) Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

- 9) The specification is objected to by the Examiner.
- 10) The drawing(s) filed on _____ is/are: a) accepted or b) objected to by the Examiner.
Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).
Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).
- 11) The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

- 12) Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).
- a) All b) Some * c) None of:
1. Certified copies of the priority documents have been received.
 2. Certified copies of the priority documents have been received in Application No. _____.
 3. Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

- 1) Notice of References Cited (PTO-892)
- 2) Notice of Draftsperson's Patent Drawing Review (PTO-948)
- 3) Information Disclosure Statement(s) (PTO-1449 or PTO/SB/08)
Paper No(s)/Mail Date _____
- 4) Interview Summary (PTO-413)
Paper No(s)/Mail Date _____
- 5) Notice of Informal Patent Application (PTO-152)
- 6) Other: _____

DETAILED ACTION

The request filed on 04/09/04 for Request for Continued Examination (RCE) under 37 CFR 1.114 based on parent Application No. 09/830,361 is acceptable and a RCE has been established. An action on the RCE follows.

Claim Rejections - 35 USC § 103

1. The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

(a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negated by the manner in which the invention was made.

2. Claims 1-3 are rejected under 35 U.S.C. 103(a) as being unpatentable over Gorczyca et al. (U. S. Patent 5,161,093) in view of Wojnarowski et al. (U. S. Patent 5,366,906).

As to claims 1, Gorczyca et al. disclose a printed circuit board (10-figure 3) comprising:

a core substrate (12, column 11, line 7) having a cavity (14, column 11, line 7), and a resin insulating layer (26; 36; 46, column 11, lines 19, 52, and column 12, line 43) and a conductor circuit (28; 38; 48) laminated on the core substrate (12), and a plurality of capacitors (IC chips 16 or electronic components capable of being as chip capacitors, column 11, line 9) are accommodated in the cavity (14).

Gorczyca et al. do not discloses an IC chip mounted on an outer layer of the conductor circuit, the IC chip being connected via a solder bump located under the IC chip, and the capacitors being located immediately below the IC chip.

Wojnarowski et al. show a wafer (10) comprising an IC chip (74) mounted on an outer layer of a conductor circuit (21), the IC chip (74) being connected via a solder bump (73), and chips (12) including an IC's and single components being located immediately below the IC chip (74).

It would have been obvious to one having ordinary skill in the art at the time the invention was made to employ an IC chip mounted on an outer layer of the conductor circuit, connected via a solder bump, and the chips being located immediately below the IC chip in the PCB of Gorczyca et al., as taught by Wojnarowski et al. for the purpose of reducing wiring inductance and power supply noise of the package.

As to claim 2, Gorczyca et al. disclose the PCB as shown in figure 3 wherein a resin (15, column 11, line 12) is charged between the plurality of capacitors in the cavity, and the resin has a thermal expansion coefficient smaller than a thermal expansion coefficient of the core substrate (column 11, lines 22-26).

As to claim 3, Gorczyca et al. discloses the PCB as shown in figure 3 wherein penetrating openings (23; 33; 43) are formed in the resin layer to form through holes.

3. Claims 4-5 are rejected under 35 U.S.C. 103(a) as being unpatentable over Gorczyca et al. ('093) in view of Wojnarowski et al. ('906), and further in view of Sunahara (U. S. Patent 6,153,290).

Gorczyca et al. and Wojnarowski et al. do not disclose a metal film including copper is formed on electrodes of the capacitor, and an electric connection for the electrodes formed with the metal film is established by plating.

Sunahara shows a PCB (9) disclosed in figures 1-4 comprising a capacitor (10), the capacitor having copper electrodes films (22, 23) on both sides of the capacitor.

It would have been obvious to one having ordinary skill in the art at the time the invention was made to employ teaching 's Sunahara in the PCB of Gorczyca and Wojnarowski in order to make electrical connection between the PCB and other components.

Allowable Subject Matter

4. Claims 6-9 are allowed.

The following is an examiner's statement of reasons for allowance: the references cited do not teach or render obvious in combination of a PCB having at least a part of electrode of each capacitor being uncoated with a coating layer and exposed to the outside, and an electric connection for the electrode exposed from the coating layer being established by plating.

Any comments considered necessary by applicant must be submitted no later than the payment of the issue fee and, to avoid processing delays, should preferably accompany the issue fee. Such submissions should be clearly labeled "Comments on Statement of Reasons for Allowance."

Response to Arguments

5. Applicant's arguments with respect to claims 1-9 have been considered but are moot in view of the new ground(s) of rejection.

Conclusion

6. The prior art made of record and not relied upon is considered pertinent to applicant's disclosure. Eichelberger, Miura et al, and Watchtler et al disclose related art.

Any inquiry concerning this communication or earlier communications from the examiner should be directed to Tuan T Dinh whose telephone number is 571-272-1929. The examiner can normally be reached on M-F.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Kammie Cuneo can be reached on 571-272-1957. The fax phone number for the organization where this application or proceeding is assigned is 703-872-9306.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see <http://pair-direct.uspto.gov>. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free).

Tuan Dinh

*Janelle Jarnie
David A. Jarnieke
Primary Exam
5/12/04*

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May 10, 2004.